

**Caroline Trippel, Assistant Professor of Computer Science & Electrical Engineering**  
Gates Computer Science Building • 353 Jane Stanford Way, Stanford, CA 94305 • [trippel@stanford.edu](mailto:trippel@stanford.edu)

ACADEMIC HISTORY

- 2013 – 2019      **Princeton University**, PhD, Computer Science  
Thesis: Concurrency and Security Verification in Heterogeneous Parallel Systems  
*ACM SIGARCH/IEEE CS TCCA Outstanding Dissertation Award*  
*CGS/ProQuest Distinguished Dissertation Award*  
Advisor: Prof. Margaret Martonosi
- 2013 – 2015      **Princeton University**, MA, Computer Science
- 2009 – 2013      **Purdue University**, BS, Computer Engineering

EMPLOYMENT RECORD

1. Jul 2020 –                      **Assistant Professor**, Computer Science and Electrical Engineering Departments                      **Stanford University**, Stanford, CA
2. Jul 2025 – Oct 2025              **Academic Consultant**, CPU Design Verification Team                      **NVIDIA**, Santa Clara, CA
3. Jun 2022 – Sep 2022              **Consultant**, SEG Formal Verification Team                      **Apple Inc.**, Cupertino, CA
4. Sep 2019 – Jul 2020              **Research Scientist**, FAIR SysML                      **Facebook**, Boston, MA
5. Sep 2013 – Sep 2019              **Research Assistant**, Computer Science Department  
Advisor: Margaret Martonosi                      **Princeton University**, Princeton, NJ
6. Su 2016 – Au 2016              **Graduate Research Intern**, Architecture Research Group                      **NVIDIA**, Westford, MA
7. Su 2015                      **Graduate Research Intern**, Architecture Research Group                      **NVIDIA**, Westford, MA
8. Su 2013                      **Verification Graduate Intern**, P-Series Verification Group                      **IBM**, Austin TX
9. Su 2012                      **Undergraduate Technical Intern**, FEV/DFT Group                      **Intel**, Hillsboro, OR
10. Su 2011                      **Undergraduate Intern**, Continuous Improvement Group                      **Blue Cross Blue Shield**, Providence, RI

AWARDS AND HONORS

1. ASPLOS 2026 Best Paper Award for CounterPoint
2. [2026 Sloan Research Fellow](#)
3. Invited Keynote at the [53rd Symposium on Principles of Programming Languages \(POPL 2026\)](#)
4. 2025 Top Pick in Hardware & Embedded Security for Serberus
5. 2025 Top Pick *Shortlist* in Hardware & Embedded Security for RTL2MμPATH
6. [2025 Google ML and Systems Junior Faculty Award](#)
7. 2024 Intel Rising Star Award
8. [OCP Silent Data Corruption Academic Research Award](#)
9. ASPLOS 2024 [Distinguished Reviewer](#)
10. HASP 2020 paper appears in: [United States National Strategy on Microelectronics Research](#)
11. [2023 Intel Outstanding Researcher Award](#)
12. Invited Keynote at the [35th International Conference on Computer Aided Verification \(CAV 2023\)](#)
13. [NSF CAREER Award](#), Division of Computing and Communication Foundations

14. 2022 Meta Research Award on [Silent Data Corruption at Scale](#)
15. 2022 [DARPA Forward Riser](#)
16. 2022 Top Pick *Shortlist* in Hardware and Embedded Security for CheckMate
17. 2021 VMware Early Career Faculty Grant
18. 2020 CGS/ProQuest Distinguished Dissertation Award
19. 2020 ACM SIGARCH/IEEE CS TCCA Outstanding Dissertation Award
20. 2018 IEEE MICRO Top Pick (top 12 Computer Architecture papers) for CheckMate
21. 2018 MIT Rising Stars in EECS Workshop
22. 2018 ACM Heidelberg Laureate Forum
23. 2017 IEEE MICRO Top Pick (top 12 Computer Architecture papers) for TriCheck
24. [2017 NVIDIA Graduate Fellow](#)
25. Au 2009 – Sp 2013 Richard E. Houser Trustee Scholarship in ECE (Purdue University, Full Tuition)
26. Au 2012 Michelle L. Ruth Memorial Scholarship (Purdue University)
27. Au 2012 Thomas A. Prewitt Memorial Scholarship (Purdue University)
28. Au 2012 Samuel David Williamson Scholarship (Purdue University)
29. Au 2012 Donald E. Knebel Electrical and Computer Engineering Scholarship (Purdue University)
30. Au 2012 – Sp 2013 Purdue University Dean’s List
31. Sp 2011 – Sp 2013 Purdue University Semester Honors
32. 2009 Intel International Science and Engineering Fair Second Place, Minor Planet named after me by MIT Lincoln Laboratory LINEAR (URL: <https://ssd.jpl.nasa.gov/sbdb.cgi#top>, search “Carolinejune”)

## PUBLICATIONS

### Refereed Conference/Symposium Proceedings

1. [FMSD26] Rachel Cleaveland and Caroline Trippel. “Formal Foundations of the MemGlue Consistency Protocol for Heterogeneous Hardware”. 2025 Formal Methods in System Design (FMSD). 2025. *(To appear - invited as one of the best papers of FMCAD24.)*
2. [ICSE26] Daniel Mendoza, Anastasia Mavridou, Andreas Katis, and Caroline Trippel. “Automating Requirements Formalization: Using LLMs and Low-Complexity Distinguishing Traces for Semantic Validation”. In Proceedings of the 48th IEEE/ACM International Conference on Software Engineering (ICSE), Rio de Janeiro, Brazil. April, 2026. *(To appear.)*
3. [ASPLOS26] Nick Lindsay, Caroline Trippel, Anurag Khandelwal, and Abhishek Bhattacharjee. “CounterPoint: Using Hardware Event Counters to Refute and Refine Microarchitectural Assumptions”. In Proceedings of the 31st International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Pittsburgh, PA. March, 2026.
4. [HPCA26] Nicholas Mosier, Hamed Nemati, John C. Mitchell, and Caroline Trippel. “Protean: A Programmable Spectre Defense”. In Proceedings of the 32nd IEEE International Symposium on High-Performance Computer Architecture (HPCA), Sydney, Australia. January-February, 2026.
5. [DIMES25] Peijing Li, Muhammad Shahir Abdurrahman, Rachel Cleaveland, Sergey Legtchenko, Philip Levis, Ioan Stefanovici, Thierry Tambe, David Tennenhouse, Caroline Trippel, and H-S Philip Wong. In Proceedings of the 3rd Workshop on Disruptive Memory Systems (DIMES), Seoul, Republic of Korea, October, 2025.

6. [Computer25] Caroline Trippel. "Specification and Formal Verification of Hardware-Software Contracts for High-Assurance Computer Architectures". IEEE Computer 58.8 (2025): 86-91.
7. [IEDM25] Shuhan Liu, Robert M Radway, Xinxin Wang, Jimin Kwon, Caroline Trippel, Philip Levis, Subhasish Mitra, and H-S Philip Wong, "Future of Memory: Massive, Diverse, Tightly Integrated with Compute - from Device to Software". 2024 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA. February, 2025.
8. [MICRO24] Yao Hsiao, Nikos Nikoleris, Artem Khyzha, Dominic P. Mulligan, Gustavo Petri, Christopher W. Fletcher, and Caroline Trippel. "RTL2M $\mu$ PATH: Multi- $\mu$ PATH Synthesis with Applications to Hardware Security Verification". In Proceedings of the 57th IEEE/ACM International Symposium on Microarchitecture (MICRO), Austin, TX. November, 2024.
9. [FMCAD24a] Rachel Cleaveland and Caroline Trippel. "Memory Consistency Model-Award Cache Coherence for Heterogeneous Hardware". In Proceedings of the 2024 Conference on Formal Methods in Computer Aided Design (FMCAD), Prague, Czech Republic. October 2024.
10. [FMCAD24b] Daniel Mendoza, Christopher Hahn, and Caroline Trippel. "Translating Natural Language to Temporal Logics with Large Language Models and Model Checkers". In Proceedings of the 2024 Conference on Formal Methods in Computer Aided Design (FMCAD), Prague, Czech Republic. October 2024.
11. [SP24] Nicholas Mosier, Hamed Nemati, John C. Mitchell, and Caroline Trippel. "Serberus: Protecting Cryptographic Code from Spectres at Compile-Time". In Proceedings of the 45th IEEE Symposium on Security & Privacy (SP), San Francisco, CA. May 2024.
12. [EuroSys24] Daniel Mendoza, Francisco Romero, and Caroline Trippel. "Model Selection for Latency-Critical Inference Serving". In Proceedings of the 10th European Conference on Computer Systems (EuroSys), Athens, Greece. April 2024.
13. [CAV23] Matthias Cosler, Christopher Hahn, Daniel Mendoza, Frederik Schmitt, and Caroline Trippel. "nl2spec: Interactively Translating Unstructured Natural Language to Temporal Logics with Large Language Models". In Proceedings of the 34th International Conference on Computer Aided Verification (CAV), Paris, France. July 2023.
14. [DAV23] Chuyue Sun, Christopher Hahn, and Caroline Trippel. "Towards Improving Verification Productivity with Circuit-Aware Translation of Natural language to SystemVerilog Assertions". 1st International Workshop on Deep Learning-aided Verification (DAV), Paris, France. July 2023.
15. [DAC23] Saranyu Chattopadhyay, Keerthikumara Devarajegowda, Bihan Zhao, Florian Lonsing, Brandon A. D'Agostino, Ioanna Vavelidou, Vijay D. Bhatt, Sebastian Prebeck, Wolfgang Ecker, Caroline Trippel, Clark Barrett, and Subhasish Mitra. "G-QED: Generalized QED Pre-silicon Verification beyond Non-Interfering Hardware Accelerators". In Proceedings of the 60th Design Automation Conference (DAC), San Francisco, CA. July, 2023.
16. [PLARCH23a] Yao Hsiao, Yasas Seneviratne, Tommy Tracy II, Kevin Skadron, and Caroline Trippel. "Design for Hardware Memory Model Verification". 1st Workshop on Programming Languages for Architecture (PLARCH), Orlando, Florida. June, 2023.
17. [PLARCH23b] Nicholas Mosier, Kate Eselius, Hamed Nemati, John C. Mitchell, and Caroline Trippel. "Hardware-Software Codesign for Mitigating Spectre". 1st Workshop on Programming

Languages for Architecture (PLARCH), Orlando, Florida. June, 2023.

18. [PLARCH23c] Paul Mure, Nathan Zhang, Caroline Trippel, Kunle Olukotun. “Tags: A Framework for Distributed Event Ordering”. 1st Workshop on Programming Languages for Architecture (PLARCH), Orlando, FL. June 2023.
19. [ISCA22] Nicholas Mosier, Hanna Lachnitt, Hamed Nemati, and Caroline Trippel. “Axiomatic Hardware-Software Contracts for Security”. In Proceedings of the 49th ACM/IEEE International Symposium on Computer Architecture (ISCA), New York, New York. June, 2022.
20. [EuroMLSys22] Daniel Mendoza and Caroline Trippel. “SLO-NNs: Service Level Objective-Aware Neural Networks”. 2nd European Workshop on Machine Learning and Systems (EuroMLSys), Rennes, France. April 2022.
21. [ASPLOS22] Geet Sethi, Bilge Acun, Niket Agarwal, Christos Kozyrakis, Caroline Trippel, and Carole-Jean Wu. “RecShard: Statistical Feature-Based Memory Optimization for Industry-Scale Neural Recommendation”. In Proceedings of the 27th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Lausanne, Switzerland. February-March, 2022.
22. [BMVC21] Deeksha Dangwal, Vincent T. Lee, Hyo Jin Kim, Tianwei Shen, Meghan Cowan, Rajvi Shah, Caroline Trippel, Brandon Reagen, Timothy Sherwood, Vasileios Balntas, Armin Alaghi, and Eddy Ilg. “Mitigating Reverse Engineering Attacks on Local Feature Descriptors”. In Proceedings of the 32nd British Machine Vision Conference (BMVC), Virtual Event. November 2021.
23. [MICRO21] Yao Hsiao, Dominic P. Mulligan, Nikos Nikoleris, Gustavo Petri, and Caroline Trippel. “Synthesizing Formal Models of Hardware from RTL for Efficient Verification of Memory Model Implementations”. In Proceedings of the 54th IEEE/ACM International Symposium on Microarchitecture (MICRO), Virtual Event. October, 2021.
24. [FMCAD21] Saranyu Chattopadhyayi, Florian Lonsing, Luca Piccolboni, Deepraj Soni, Peng Wei, Xiaofan Zhang, Yuan Zhou, Luca Carloni, Deming Chen, Jason Cong, Ramesh Karri, Zhiru Zhang, Caroline Trippel, Clark Barrett, and Subhasish Mitra. “Scaling Up Hardware Accelerator Verification using A-QED with Functional Decomposition”. In Proceedings of the 2021 Conference on Formal Methods in Computer Aided Design (FMCAD), Virtual Event. October 2021.
25. [ISCA21] Jose Rodrigo Sanchez Vicarte, Pradyumna Shome, Nandeeka Nayak, Caroline Trippel, Adam Morrison, David Kohlbrenner, and Christopher W. Fletcher. “Opening Pandora’s Box: A Systematic Study of New Ways Microarchitecture Can Leak Private Data”. In Proceedings of the 48th ACM/IEEE International Symposium on Computer Architecture (ISCA), Virtual Event. June 2021.
26. [PLDI21] Meghan Cowan, Deeksha Dangwal, Armin Alaghi, Caroline Trippel, Vincent T. Lee, and Brandon Reagen. “Porcupine: A Synthesizing Compiler for Vectorized Homomorphic Encryption”. In Proceedings of the 42nd ACM SIGPLAN International Conference on Programming Language Design and Implementation (PLDI), Virtual Event. June 2021.
27. [ASPLOS21] Mark Wilkening, Udit Gupta, Samuel Hsia, Caroline Trippel, Carole-Jean Wu, David Brooks, and Gu-Yeon Wei. “RecSSD: Near Data Processing for Solid State Drive Based Recommendation Inference”. In Proceedings of the 26th International Conference on Architectural

Support for Programming Languages and Operating Systems (ASPLOS), Virtual Event. April 2021.

28. [MLSys21] Kiwan Maeng, Shivam Bharuka, Isabel Gao, Mark Jeffrey, Vikram Saraph, Bor-Yiing Su, Caroline Trippel, Jiyan Yang, Mike Rabbat, Brandon Lucia, and Carole-Jean Wu. “Understanding and Improving Failure Tolerant Training for Deep Learning Recommendation with Partial Recovery”. In Proceedings of the 3rd Conference on Machine Learning and Systems (MLSys), Virtual Event. April 2021.
29. [HASP20] Deeksha Dangwal, Meghan Cowan, Armin Alaghi, Vincent T. Lee, Brandon Reagen, and Caroline Trippel. “SoK: Opportunities for Software-Hardware-Security Codesign for Next Generation Secure Computing”. In Proceedings of the 9th ACM Workshop on Hardware and Architectural Support for Security and Privacy (HASP), Virtual Event. October 2020.
30. [ISCA20] Naorin Hossain\*, Caroline Trippel\*, and Margaret Martonosi. “TransForm: Formally Specifying Transistency Models and Synthesizing Enhanced Litmus Tests”. In Proceedings of the 47th ACM/IEEE International Symposium on Computer Architecture (ISCA), Virtual Event. May-June 2020. \*The first two authors contributed equally.

*Presents an axiomatic vocabulary for formally specifying “transistency models” and a tool for synthesizing litmus tests enhanced with transistency features, when supplied with a formal transistency model specification.*

31. [TopPicks19] Caroline Trippel, Daniel Lustig, and Margaret Martonosi. “Security Verification through Automatic Hardware-Aware Exploit Synthesis: The CheckMate Approach”. IEEE Micro: Top Picks from the Computer Architecture Conferences of 2018, vol. 39, no. 3, pp. 84-93, May-June 2019.

*Makes the important observation that MCM analysis is in many ways similar to hardware security analysis, paving the way for fresh approaches to security specification and verification in the hardware-software stack.*

32. [FMCAD18] Hongce Zhang, Caroline Trippel, Yatin A. Manerkar, Aarti Gupta, Margaret Martonosi, and Sharad Malik. “Integrating Memory Consistency Models with Instruction-Level Abstractions for Heterogeneous System-onChip Verification”. In Proceedings of the 2018 Conference on Formal Methods in Computer Aided Design (FMCAD), Austin, Texas. October-November 2018.

*New approach for integrating axiomatic memory consistency model specifications with operational specifications of heterogeneous SoC components to reason about overall system behavior.*

33. [MICRO18] Caroline Trippel, Daniel Lustig, and Margaret Martonosi. “CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests”. In Proceedings of the 51st IEEE/ACM International Symposium on Microarchitecture (MICRO), Fukuoka, Japan. October 2018.

*Automated approach/ tool for evaluating microarchitectural susceptibility to exploit classes and synthesizing proof-of-concept exploit code; CheckMate synthesized Meltdown, Spectre, new attacks.*

34. [TopPicks18] Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. “Full-Stack Memory Consistency Model Verification with TriCheck”. IEEE Micro: Top Picks from the Computer Architecture Conferences of 2017, vol. 38, no. 3, pp. 58-68, May-June 2018.

*First full-stack language/ISA/microarchitecture memory consistency model verification tool, which uncovered concrete and fundamental problems in the C11/C++11 and RISC-V memory models.*

35. [ASPLOS17] Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. “TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA”. In Proceedings of the 22nd ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Xi’an, China. April 2017.

*Established the value of full-stack memory consistency model verification and highlighted issues with the RISC-V memory model that were subsequently fixed through the RISC-V Memory Model Working Group.*

36. [ISCA15] Daniel Lustig, Caroline Trippel, Michael Pellauer, and Margaret Martonosi. “ArMOR: Defending Against Memory Consistency Model Mismatches in Heterogeneous Architectures”. In Proceedings of the 42nd ACM/IEEE International Symposium on Computer Architecture (ISCA), Portland, Oregon. June, 2015.

*Framework that supports specifying, algorithmically reasoning about, and automatically translating between heterogeneous MCMs.*

#### Non-refereed Publications

1. [ARXIV26] Yuheng Wu, Berk Gokmen, Zhouhua Xie, Peijing Li, Caroline Trippel, Priyanka Raina, and Thierry Tambe, “LLM-FSM: Scaling Large Language Models for Finite-State Reasoning in RTL Code Generation”. arXiv, abs/2602.07032. February, 2026.
2. [OSCAR25] Yao Hsiao, Nikos Nikoleris, Artem Khyzha, Dominic P. Mulligan, Gustavo Petri, Christopher W. Fletcher, and Caroline Trippel. “Automatically Uncovering Hardware Side-Channels in Processor RTL with Multi- $\mu$ PATH Synthesis”. 4th Workshop on Open-Source Computer Architecture Research (OSCAR), New York, New York. June, 2025.
3. [OSCAR25] Nicholas Mosier, Hamed Nemati, John Mitchell and Caroline Trippel. “Fast, Accurate, and Novel Performance Evaluations with PinCPU”. 4th Workshop on Open-Source Computer Architecture Research (OSCAR), New York, New York. June, 2025.
4. [ARXIV25a] Anjiang Wei, Huanmi Tan, Tarun Suresh, Daniel Mendoza, Thiago SFX Teixeira, Ke Wang, Caroline Trippel, and Alex Aiken. “VeriCoder: Enhancing LLM-Based RTL Code Generation through Functional Correctness Validation”. April 2025.
5. [ARXIV25b] Nicholas Mosier, Hamed Nemati, John C. Mitchell, and Caroline Trippel. “Analyzing and Exploiting Branch Mispredictions in Microcode”. January 2025.
6. [DAM24] Mark Horowitz, Philip Levis, Subhasish Mitra, Thierry Tambe, Caroline Trippel, Keith Winstein, H.-S. Philip Wong, and Mary Wootters. “DAM: Differentiated Access Memory Systems and Applications”. April 2024.
7. [ARXIV24] Abhinav Lalwani, Lovish Chopra, Christopher Hahn, Caroline Trippel, Zhijing Jin, and Mrinmaya Sachan. “NL2FOL: Translating Natural Language to First-Order Logic for Logical

Fallacy Detection”. arXiv, abs/2405.02318. April 2024.

8. [OSCAR22] Yao Hsiao, Dominic P. Mulligan, Nikos Nikoleris, Gustavo Petri, and Caroline Trippel. “Scalable Assurance via Verifiable Hardware-Software Contracts”. 1st Workshop on Open-Source Computer Architecture Research (OSCAR), New York, New York. June, 2022.
9. [ARXIV22] Daniel Mendoza and Caroline Trippel. “Dynamic Network Adaptation at Inference”. arXiv, abs/2204.08400. April 2022.
10. [ARXIV21] Nicholas Mosier, Hanna Lachnitt, Hamed Nemati, and Caroline Trippel. “Relational Models of Microarchitectures for Formal Security Analyses”. arXiv, abs/2112.10511. December 2021.
11. [ARXIV21] Deeksha Dangwal, Vincent T Lee, Hyo Jin Kim, Tianwei Shen, Meghan Cowan, Rajvi Shah, Caroline Trippel, and Brandon Reagen, Timothy Sherwood, Vasileios Balntas, Armin Alaghi, and Eddy Ilg. “Analysis and Mitigations of Reverse Engineering Attacks on Local Feature Descriptors”. arXiv, abs/2105.03812. December 2021.
12. [PrincetonUniversity19] Caroline Trippel. “Concurrency and Security Verification in Heterogeneous Parallel Systems.” PhD Dissertation. Princeton University. November 2019.

*Despite parallelism and heterogeneity being around for a long time, the degree to which both are being simultaneously deployed poses grand challenge problems in computer architecture regarding ensuring the accuracy of event orderings and interleavings in system-wide executions. As it turns out, event orderings form the cornerstone of correctness (e.g., memory consistency models) and security (e.g., speculation-based hardware exploits) in modern processors. Thus, my thesis work creates formal, automated techniques for specifying and verifying the accuracy of event orderings for programs running on heterogeneous, parallel systems to improve their correctness and security.*

13. [ARXIV18] Caroline Trippel, Daniel Lustig, and Margaret Martonosi. “MeltdownPrime and SpectrePrime: Automatically-Synthesized Attacks Exploiting Invalidation-Based Coherence Protocols”. arXiv, abs/1802.03802. February 2018.

*Overview of MeltdownPrime and SpectrePrime exploits that were automatically synthesized by CheckMate and which were demonstrated to leak private data on Intel hardware.*

14. [ARXIV16] Yatin A. Manerkar, Caroline Trippel, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. “Counterexamples and Proof Loophole for the C/C++ to POWER and ARMv7 Trailing-Sync Compiler Mappings”. arXiv, abs/1611.01507. November 2016.

*Identification of an error in a compiler mapping proof from C11 to the IBM Power and ARMv7 ISAs; the error is what enabled TriCheck to identify concrete compiler mapping counterexamples.*

15. [ARXIV16] Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. “Exploring the Trisection of Software, Hardware, and ISA in Memory Model Design”. arXiv, abs/1608.07547. August 2016.

## Blog Posts

1. [SIGARCH23] Caroline Trippel. [Interactively Translating Unstructured Natural Language to Temporal Logics with nl2spec](#). SIGARCH Blog. Jun 2023.
2. [SIGARCH22] Caroline Trippel. [Silent Data Corruption at Scale](#). SIGARCH Blog. Aug 2022.
3. [SIGARCH21] Caroline Trippel. [Applications of Formal Methods in Computer Architecture.](#)” SIGARCH Blog. Sept 2021.
4. [SIGARCH20a] Caroline Trippel. [The Academic Job Search: A Memoir, Part 2](#). SIGARCH Blog, Dec 2020.
5. [SIGARCH20b] Caroline Trippel. [The Academic Job Search: A Memoir](#). SIGARCH Blog. Dec 2020.
6. [SIGARCH20c] Caroline Trippel. [Reflections on the ISCA Mini-Panel on Security](#). SIGARCH Blog. Aug 2020.

## PATENTS

Patents under consideration by the USPTO:

18/541,722 United States

Filed December 15, 2023

GENERALIZED QED PRE-SILICON VERIFICATION FRAMEWORK

Subhasish Mitra, Clark Barrett, Caroline Trippel, Saranyu Chattopadhyay

Stanford S22-526

1126-086

## PROFESSIONAL ACTIVITIES

- |     |        |  |                           |
|-----|--------|--|---------------------------|
| 1.  | 2020 – | ACM  | Member                    |
| 2.  | 2020 – | ACM SIGARCH Blog   | Contributor               |
| 3.  | 2022 – | IEEE   | Member                    |
| 4.  | 2024 – | Stanford Differentiated Access Memories (DAM) Project  | Co-Director               |
| 5.  | 2025   | Communications of the ACM (CACM) <a href="#">Reviewer Board Project</a>                                | Review Board Member       |
| 6.  | 2025   | ISCA 2026  | TPC                       |
| 7.  | 2025   | HPCA 2026  | TPC                       |
| 8.  | 2025   | ISCA 2025  | Session Chair             |
| 9.  | 2025   | Open-Source Computer Architecture Research (OSCAR) Workshop, at ISCA 2025                              | Organizing Committee, TPC |
| 10. | 2025   | Young Architects Workshop (YArch), at ASPLOS 2025  | Co-Organizer              |
| 11. | 2025   | ISCA 2025  | TPC                       |
| 12. | 2024   | “Applying to Graduate School” panel, Undergrad Architectural Mentoring Workshop (uArch), at MICRO 2024 | Panelist                  |
| 13. | 2024   | Meet a Senior Architect, at MICRO 2024   | Mentor                    |
| 14. | 2024   | Top Picks in Hardware and Embedded Security (HES), at ICCAD 2024                                       | TPC                       |
| 15. | 2024   | Open-Source Computer Architecture Research (OSCAR) Workshop, at ISCA 2024                              | Organizing Committee, TPC |

16.	2024	Young Architects Workshop (YArch), at ASPLOS 2024	Co-Organizer
17.	2023	Dagstuhl Seminar 23481, “MAD: Microarchitectural Attacks and Defenses”	Participant
18.	2023	ACM Student Research Competition (SRC), at MICRO 2023	Co-Chair
19.	2023	Programming Languages for Architecture (PLARCH) Workshop, at FCRC 2024	Organizing Committee, TPC
20.	2023	Undergrad Architecture Mentoring Workshop, at ISCA 2023	Mentor
21.	2023	Meet a Senior Architect, at ISCA 2023	Mentor
22.	2023	ASPLOS 2024, Winter	TPC
23.	2023	ASPLOS 2024, Summer	TPC
24.	2023	ASPLOS 2024, Spring	TPC
25.	2023	IEEE Micro Top Picks 2023	TPC
26.	2022	Top Picks in Hardware and Embedded Security (HES), at ICCAD 2022	TPC
27.	2022	HPCA 2023	ERC
28.	2022	Northwestern Cross-layer Computing Summer School: Circuits to System	Mentor
29.	2022	Stanford-Berkeley Research Meetup for Women in CS/EE	Panelist
30.	2022	Berkeley/Stanford/UCSC Cloud Workshop, part of the <a href="#">Industry-Academia Partnership</a>	Co-Organizer
31.	2022	Wild and Crazy Ideas (WACI) Workshop, at ASPLOS 2022	Co-Organizer, TPC
32.	2022	NSF CISE/CCF workshop “Redefining the Future of Computer Architecture from First Principles (Arch-1)”	Participant (1/~31)
33.	2022	ASPLOS 2023, Winter	TPC
34.	2022	ASPLOS 2023, Summer	TPC
35.	2022	ASPLOS 2023, Spring	TPC
36.	2022	OSDI 2022	Expert Reviewer
37.	2021	Meet a Senior Architect, at ISCA 2021	Mentor
38.	2021	EuroSys Doctoral Workshop, at EuroSys 2021	TPC, Mentor
39.	2021	Young Architects Workshop (YArch), at ASPLOS 2021	TPC, Mentor
40.	2021	ISCA 2021	TPC
41.	2021	IEEE Micro Top Picks 2021	TPC
42.	2021	MLSys 2022	TPC
43.	2021	ASPLOS 2022	TPC
44.	2021	Workshops and Tutorials, at ASPLOS 2021	Co-Chair
45.	2020	JOBS Workshop, at MICRO 2020	Panelist
46.	2020	Career Workshop for Inclusion and Diversity in Computer Architecture (CWIDCA), at MICRO 2020	Panelist
47.	2020	ACM Student Research Competition (SRC), at MICRO 2020	TPC
48.	2020	Hardware and Architectural Support for Security and Privacy (HASP) Workshop, at MICRO 2020	TPC
49.	2020	Meet a Senior Architect, at ISCA 2020	Mentor
50.	2020	ASPLOS 2021	TPC
51.	2020	DARPA/ISAT Study on “DOPLR: Data-Oblivious Interdisciplinary Representation”	Participant (1/~45)
52.	2020	NSF Arch+HPC Panel P201446	Reviewers
53.	2020	ISCA 2020 Industry Track	TPC
54.	2019	ASPLOS 2020	TPC
55.	2019	MICRO 2019	TPC

56.	2018	“Principles of Secure Processor Architecture Design” by Jakub Szefer, a Morgan & Claypool Synthesis Lecture on Computer Architecture	Expert Reviewer
57.	2018	International Symposium on Memory Management	Expert Reviewer
58.	2016 – 2017	RISC-V Memory Model Working Group	Member
59.	2016	Dagstuhl Seminar 16471, “Concurrency with Weak Memory Models: Semantics, Languages, Compilation, Verification, Static Analysis, and Synthesis”	Participant
60.	2013-2019	Princeton Society of Women Engineers (SWE)	Member
61.	2013-2019	Princeton Women in Computer Science (PWICS)	Member

#### UNIVERSITY AND DEPARTMENTAL SERVICE

1.	2020 –	Stanford Women in EE, Mentor	
2.	Au 2025	Stanford CS 300 Seminar: “High Assurance Computer Architectures”	
3.	Au 2025	Stanford EE 301 Seminar: “High Assurance Computer Architectures”	
4.	Su 2025	CURIS Student Research Advisor x2	
5.	AY 2024/25	CS PhD Graduate Admissions Committee, Systems Area Co-Lead	
6.	AY 2024/25	EE Student Life Committee, Faculty Chair	
7.	AY 2024/25	EE PhD Graduate Admissions Reader	
8.	Au 2024	Stanford CS 300 Seminar: “High Assurance Computer Architectures”	
9.	Au 2024	Stanford EE 301 Seminar: “High Assurance Computer Architectures”	
10.	Au 2023	Stanford CS 300 Seminar: “Verified Software Security Down to Gates”	
11.	Au 2023	Stanford EE 301 Seminar: “Verified Software Security Down to Gates”	
12.	Au 2023	CS 257 offered via the Stanford Engineering Center for Global and Online Learning (CGOE, formerly SCPD)	
13.	Wi 2023	EE 282 offered via the Stanford Engineering Center for Global and Online Learning (CGOE, formerly SCPD)	
14.	AY 2021/22 – AY 2022/23	Stanford Diversifying Academia, Recruiting Excellence (DARE) Program, Faculty Resource Advisor to EE PhD Student Francisco Romero	
15.	AY 2022/23	CS PhD Graduate Admissions Committee, Systems Area Co-Lead	
16.	AY 2022/23	EE Student Life Committee	
17.	AY 2022/23	EE PhD Graduate Admissions Reader	
18.	Au 2022	Stanford EE 301 Seminar: “Scalable Assurance via Verifiable Hardware-Software Contracts”	
19.	Au 2022	EE Student Roundtable	
20.	Wi 2022	EE 282 offered via the Stanford Engineering Center for Global and Online Learning (CGOE, formerly SCPD)	
21.	AY 2021/22	CS PhD Graduate Admissions Committee, Systems Area Lead	
22.	AY 2021/22	EE Student Life Committee	
23.	AY 2021/22	EE PhD Graduate Admissions Reader	
24.	Au 2021	Stanford CS 300 Seminar: “Formally Verifying Hardware with Happens-Before Analysis”	
25.	Au 2021	Stanford EE 301 Seminar: “Formally Verifying Hardware with Happens-Before Analysis”	
26.	Wi 2021	Stanford CS Academic Job Market Panel	
27.	Wi 2021	EE 282 offered via the Stanford Engineering Center for Global and Online Learning (CGOE, formerly SCPD)	
28.	2020/21	CS PhD Graduate Admissions Committee, Systems	

- 29. Au 2020 Stanford CS 300 Seminar: “Application Reliability and Security via Formal Methods for Systems”
- 30. Au 2020 Stanford EE 301 Seminar: “Application Reliability and Security via Formal Methods for Systems”

## PRESENTATIONS

### Invited Plenary Talks and Distinguished Lectures

- 1. Jan 2026 Hardware-Software Contracts for High Assurance with Applications to Side-Channel Security 53rd ACM SIGPLAN Symposium on Principles of Programming Languages (POPL), Rennes, France. Hosts: Sandrine Blazy, Suresh Jagannathan
- 2. Oct 2025 Automated and Scalable Hardware Side Channel Discovery with Property Decomposition and Model Checkers Jasper User Group (JUG) 2025 Host: Vigyan Singal
- 3. Oct 2025 Design and Formal Verification of Hardware-Software Security Contracts 17th International Conference on Verified Software: Theories, Tools, and Experiments (VSTTE), Menlo Park, CA, USA. Hosts: Clement Pit-Claudel, Katherine Kosaian
- 4. Jul 2023 Verified Software Security Down to Gates 35th International Conference on Computer Aided Verification (CAV), Paris, France. Hosts: Constantin Enea, Akash Lal

### Other Invited Presentations

- 1. Oct 2025 Seed Grant Presentation: Democratizing Hard Hardware-Specification Verification Tasks 2025 Stanford SystemX Fall Conference Talk
- 2. Oct 2025 Automated Property Generation for Hardware Verification Alphabet Talk Host: Adriana Maggiore
- 3. Sep 2025 Scalable Hardware Side-Channel Discovery with Property Decomposition and Model Checkers Stanford Center for Automated Reasoning (CENTAUR) Annual Meeting Talk Host: Clark Barrett
- 4. Sep 2025 Ep 21: High-assurance Computer Architectures with Dr. Caroline Trippel, Stanford University Computer Architecture Podcast Podcast Hosts: Svinay Subramanian, Lisa Hsu
- 5. Sep 2025 Design and Formal Verification of Hardware Side-Channel Defenses Intel Academic Conference Talk Host: Matthias Schunter
- 6. Aug 2025 AI-Driven, Formal Verification-Guided Hardware Design Google AI-Driven Chip Design Workshop Talk Host: Partha Ranganathan

7.	Aug 2025	Hardware-Software Cooperation Against Spectre Attacks	Apple	Talk	Host: John Pape
8.	Aug 2025	Hardware-Software Cooperation Against Spectre Attacks	SRI	Talk	Host: Mark Mitchell
9.	Nov 2024	Translating Natural Language to Temporal Logics with Large Language Models and Model Checkers	AI4HW & HW4AI Workshop, at MICRO 2024	Talk	Host: Yingyan (Celine) Lin
10.	Oct 2024	RTL2M $\mu$ PATH: Multi- $\mu$ PATH Synthesis with Applications to Hardware Security Verification	NVIDIA	Talk	Host: Vigyan Singhal
11.	Sep 2024	Verified Software Security Down to Gates	Intel Scalable Assurance Fall Workshop	Talk	Host: Matthias Schunter
12.	Jul 2024	Mobilizing Hardware and Software Towards SDC Testing, Detection, & Correction	OCP Silent Data Corruption Academic Research Award Kickoff Meeting	Talk	Host: Bharath Parthasarathy
13.	Jul 2024	Multi- $\mu$ PATH Synthesis with Applications to Hardware Security Verification	NVIDIA	Talk	Host: David Nellans
14.	May 2024	Orchestrating Coherence and Consistency in Heterogeneous Shared Memory Systems	Stanford Differentiated Access Memories (DAM) Kickoff Workshop	Talk	Hosts: Phil Levis and Caroline Trippel
15.	Dec 2023	Verified Software Security Down to Gates	Dagstuhl Seminar 23481, "MAD: Microarchitectural Attacks and Defenses"	Talk	Hosts: Christopher Fletcher, Marco Guanieri, David Kohlbrenner, and Cl��mentine Maurice
16.	Nov 2023	Verified Software Security Down to Gates	Stanford SystemX Fall Conference	Talk	
17.	Sep 2023	Verified Software Security Down to Gates	Intel Scalable Assurance Fall Workshop	Talk	Host: Matthias Schunter
18.	Jul 2023	System-Level Testing for Silent Data Corruptions	Open Compute Project Bi-Weekly Meeting	Talk	Host: Bharath Parthasarathy
19.	Jun 2023	Round Table on Implications for the Design and Validation of Secure Systems	7th Workshop on Computer Architecture Research with RISC-V (CARRV), at ISCA 2023	Panelist	Host: Trevor Carlson
20.	Jun 2023	Uncovering Transmitter Instructions on the RISC-V CVA6 Processor	7th Workshop on Computer Architecture Research with	Talk	Host: Trevor Carlson

21.	Jun 2023	Scalable Assurance via Verifiable Hardware-Software Contract	RISC-V (CARRV), at ISCA 2023 Council on Electronic Design Automation (CEDA) Hong Kong Chapter, 2023 Seminar Series	Talk	Host: Hongce Zhang
22.	May 2023	Scalable Assurance via Verifiable Hardware-Software Contracts	Intel Scalable Assurance Spring Workshop	Talk	Host: Matthias Schunter
23.	Mar 2023	Searching for Bugs in Real Computer Systems	Women in Computer Architecture (WICARCH) Webinar	Talk	
24.	Feb 2023	Scalable Assurance via Verifiable Hardware-Software Contracts	Intel IPAS Tech Sharing Seminar	Talk	Host: Sayak Ray
25.	Feb 2023	Scalable Assurance via Verifiable Hardware-Software Contracts	Workshop on Security for Custom Computing Machines (SCCM), at FPGA 2023	Talk	Hosts: Dustin Richmond, Ryan Kastner, Jeff Goeders, Mirjana Stojilović
26.	Jan 2023	Scalable Assurance via Verifiable Hardware Software Contracts	Stanford Engineering Research Introductions ( <a href="#">SERIS</a> ) Program	Talk	
27.	Jun 2022	Panel on Silent Data Corruption	ISCA 2022	Panelist	
28.	Nov 2022	System-Level Testing for Silent Data Corruptions	AMD	Talk	Host: Sudhanva Gurumurthi
29.	Sep 2022	Scalable Assurance via Formal and Verifiable Hardware-Software Contracts	Intel Scalable Assurance Fall Workshop	Talk	Host: Matthias Schunter
30.	Aug 2022	System-Level Testing for Silent Data Corruptions	2022 Google Accelerators, Compute, Reliability, Security (ACRS) Workshop	Talk	Host: Parthasarathy Ranganathan
31.	Jul 2022	Scalable Assurance via Formal and Verifiable Security Contracts	Stanford Center for Automated Reasoning (CENTAUR) Annual Meeting	Talk	Host: Clark Barrett
32.	Jun 2022	System-Level Testing for Silent Data Corruptions	Google	Talk	Host: Bharath Parthasarathy
33.	Nov 2021	Formally Verifying Hardware with Happens-Before Analysis	2021 Stanford SystemX Fall Conference	Talk	
34.	Oct 2021	Synthesizing Formal Models of Hardware from RTL for	AHA Affiliates Meeting	Talk	Host: Priyanka Raina, Mark Horowitz

35.	Oct 2021	Efficient Hardware Memory Model and Security Verification Automatically Synthesizing Formal Processor Models from RTL for Scalable Hardware Security Verification	Intel Scalable Assurance Program Kickoff	Talk	Host: Matthias Schunter
36.	Sep 2021	Application Correctness and Security via Formal Methods for Systems	VMWare	Talk	Host: Jayneel Gandhi
37.	Sep 2021	Formally Evaluating Microarchitectural Security with Happens-Before Analysis	Stanford Security Forum	Talk	Hosts: Dan Boneh, Zakir Durumeric
38.	Aug 2021	Searching for Bugs in Real Computer Systems	2021 Cross-layer Computing Summer School: Circuits to System	Talk	Hosts: Jie Gu, Russ Joseph, Seda Memik, Qi Zhu
39.	Aug 2021	Preparing for an Academic Career	2021 Cross-layer Computing Summer School: Circuits to System	Panelist	Hosts: Jie Gu, Russ Joseph, Seda Memik, Qi Zhu
40.	Jun 2021	Application Correctness & Security via Formal Methods for Systems	Apple	Talk	Host: Abhishek Datta
41.	Jun 2021	Application Correctness & Security via Formal Methods for Systems	Intel/Stanford Research Collaboration Meeting	Talk	
42.	Apr 2021	Searching for Bugs in Real Computer Systems	Workshop on Negative results, Opportunities, Perspectives, and Experiences (NOPE), at ASPLOS 2021	Talk	Hosts: Lillian Pentecost, Udit Gupta, David Brooks, Brandon Reagen, Svilen Kanev, Bob Adolf
43.	Nov 2020	Lifting Axiomatic Hardware Specifications from RTL for Security Analysis	Intel Side-Channel Academic Program (SCAP) Fall Workshop	Talk	Host: Matthias Schunter
44.	Nov 2020	Application Reliability and Security via Formal Methods for Systems	2020 Stanford SystemX Fall Conference	Talk	
45.	Oct 2020	My Academic Interview Tips	JOBS Workshop, at MICRO 2020	Talk	Hosts: Akshitha Sriraman, Akanksha Jain, Aporva Amarnath, Emily Ruppel
46.	Aug 2020	Application Reliability and Security via Formal Methods for Systems	2020 Annual Meeting, Stanford Computer Forum,	Talk	

			New Research Directions in CS Session		
47.	Jun 2020	Security Mini-Panel	ISCA 2020	Panelist	
48.	Jan 2020	My Academic Interview Tips and An Intro to My Research	Women in Computer Architecture (WICARCH) Webinar	Talk	
49.	Sep 2019	Synthesizing Security Exploits	2019 State-of-the-Art in Program Synthesis Workshop Microsoft	Talk	Hosts: Saurabh Srvastava, Ratislav Bodik Host: Doug Berger
50.	Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings		Talk	
51.	Nov 2018	Concurrency and Security Verification in Heterogeneous Parallel Systems	2018 IBM Workshop on Architectures for Secure, Cognitive, and Datacenter Computing MIT CSAIL	Talk	Hosts: Michael Healy, Arvind Kumar
52.	Nov 2018	Concurrency and Security Verification in Heterogeneous Parallel Systems		Talk	Host: Saman Amarasinghe
53.	Mar 2018	Automated Exploit Program Generation for Hardware Security Verification	Apple Security Engineering and Architecture Group Grad Fellow	Talk	Host: Ivan Krstić
54.	Mar 2018	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	FastForward Session, at NVIDIA GPU Technology Conference (GTC)	Talk	
55.	Mar 2018	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	Grad Fellow FastForward Session, at NVIDIA GPU Technology Conference (GTC)	Poster	
56.	Sep 2017	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	2017 SRC TECHCON	Talk	
57.	Sep 2017	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	2017 SRC TECHCON	Poster	
58.	Jul 2017	Why Memory Consistency Models Matter in a World of Parallelism and Shared Memory	Rutgers University DIMACS Research Experiences for Undergraduates SRI International	Talk	Host: Lazaros Gallos
59.	Nov 2016	TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA		Talk	Host: Prashanth Mundkur

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| 60. | Sep 2016 | Memory Consistency Model<br>Aware ISA Design and<br>Specification | 2016 SRC<br>TECHCON | Talk   |
| 61. | Sep 2016 | Memory Consistency Model<br>Aware ISA Design and<br>Specification | 2016 SRC<br>TECHCON | Poster |

#### Contributed Conference Presentations

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|-----|----------|---|--|----------|---|
| 1.  | Apr 2024 | SynthLC: Synthesizing Verified Leakage Contracts from SystemVerilog Processor Designs   |  | Talk     | 2024 New England Systems Verification Day Workshop  |
| 2.  | Dec 2022 | Scalable Assurance via Formal and Verifiable Hardware- Software Contracts   |  | Poster   | DARPA Risers Workshop, at 2022 DARPA Forward Conference   |
| 3.  | Nov 2022 | Microarchitectural Attack Synthesis with Happens-Before Analysis  |  | Talk     | Top Picks in Hardware and Embedded Security (HES) Workshop, at ICCAD 2022                                       |
| 4.  | Jan 2021 | Concurrency and Security Verification in Heterogeneous Parallel Systems   |  | Talk     | Phil Harper Lapidus Lecture/CGS Awards Ceremony   |
| 5.  | Sep 2019 | CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests   |  | Talk     | 2019 Arm Summit   |
| 6.  | Jun 2019 | Demystifying Memory Models Across the Computing Stack<br><i>Authors: Yatin A. Manerkar, Caroline Trippel, Margaret Martonosi</i>                                    |  | Tutorial | ISCA 2019   |
| 7.  | Oct 2018 | CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests   |  | Talk     | MICRO 2018  |
| 8.  | Oct 2018 | CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests   |  | Poster   | MICRO 2018  |
| 9.  | Sep 2018 | Concurrency and Security Verification in Heterogeneous Parallel Systems   |  | Poster   | 2018 Heidelberg Laureate Forum  |
| 10. | Jun 2018 | Why Memory Consistency Models Matter... And tools for analyzing and verifying them.<br><i>Authors: Caroline Trippel and Yatin A. Manerkar</i>                       |  | Tutorial | 2018 Uppsala Programming for Multicore Architectures Research Center (UPMARC) Multicore Computing Summer School |
| 11. | Jun 2017 | Why Memory Consistency Models Matter... And tools for analyzing and verifying them.<br><i>Authors: Yatin A. Manerkar, Caroline Trippel, and Margaret Martonosi.</i> |  | Tutorial | ISCA 2017   |
| 12. | Apr 2017 | TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA  |  | Talk     | ASPLOS 2017   |
| 13. | Apr 2017 | TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA  |  | Poster   | ASPLOS 2017   |

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| 14. Nov 2016 | A Memory Consistency Model for RISC-V   | Talk   | 5th RISC-V Workshop  |
| 15. Apr 2016 | Design Space Exploration Techniques for Memory Consistency Model Aware ISA Specification    | Poster | CRA-W Grad Cohort  |
| 16. Dec 2015 | ArMOR: Defending Against Memory Consistency Model Mismatches in Heterogeneous Architectures | Poster | Career Workshop for Inclusion and Diversity in Computer Architecture (CWIDCA), at MICRO 2015 |

#### Department Seminars

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|--------------|---|---|--|
| 1. Oct 2025  | Hardware-Software Cooperation Against Side-Channel Attacks  | UC Berkeley, Sky Seminar  | Host: Sky Computing Lab  |
| 2. Jun 2025  | Design and Formal Verification of Hardware-Software Security Contracts                            | EPFL, Summer Research Institute 2025                                    | Hosts: Clément Pit-Claudel, Haitham Al Hassanieh, Mathias Payer, Sanidhya Kashyap, Thomas Bourgeat |
| 3. Mar 2025  | Towards High Assurance Computer Architectures   | USC Symposium on the Future of Computing: A 25-Year Vision              | Host: Murali Annavaram   |
| 4. Nov 2024  | RTL2M $\mu$ PATH: Multi- $\mu$ PATH Synthesis with Applications to Hardware Security Verification | Duke University, Advanced Computer Architecture I Course                | Host: Lisa Wu Wills  |
| 5. Nov 2024  | RTL2M $\mu$ PATH: Multi- $\mu$ PATH Synthesis with Applications to Hardware Security Verification | Duke University, Advanced Computer Architecture Course                  | Host: Lisa Wu Wills  |
| 6. Nov 2024  | Automatically Uncovering Hardware Side-Channels in Processor RTL with Multi- $\mu$ PATH Synthesis | Graz University of Technology   | Host: Roderick Bloem   |
| 7. Jun 2024  | Verified Software Security Down to Gates  | 2024 MPI-SP Symposium on Systems Security                               | Host: Peter Schwabe  |
| 8. Oct 2023  | Silent Data Corruptions at Scale: New Horizons or Familiar Foes?                                  | University of Michigan, Advanced Topics in Computer Architecture Course | Host: Todd Austin  |
| 9. Apr 2022  | Scalable Assurance via Formal and Verifiable Hardware-Software Contracts                          | Berkeley Security Seminar   | Host: Emma Dauterman   |
| 10. May 2021 | Application Correctness & Security via Formal Methods for Systems                                 | Stanford Systems Seminar  | CS   |
| 11. Apr 2021 | Verifying Correctness and Security of Hardware through Event Orderings                            | Brown University, Logic for Systems Course                              | Host: Timothy Nelson   |
| 12. Dec 2020 | Application Security via Formal Methods for Systems   | Stanford Security Lunch   | CS   |
| 13. Oct 2019 | Concurrency and Security Verification in Heterogeneous Parallel Systems                           | Princeton University Preliminary Final Public Oral (FPO)                | CS   |

14. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Brown University	CS
15. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	University of California, Berkeley	EECS
16. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	University of California, Santa Barbara	CS
17. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Carnegie Mellon University	ECE, CS
18. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Columbia University	CS
19. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Cornell University	CS
20. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Cornell Tech	ECE
21. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Duke University	CS, ECE
22. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	University of Illinois Urbana-Champaign	CS
23. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Northeastern University	CS, ECE
24. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	University of Pennsylvania	CS
25. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Stanford University	CS
26. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	University of Texas at Austin	CS
27. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Tufts	ECE
28. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	University of Washington	CS
29. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	University of Wisconsin-Madison	CS, ECE
30. Sp 2019	Made to Order: Verifying Correctness and Security of Hardware through Event Orderings	Yale University	CS

31. Mar 2018	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	Brown University	CS
32. Sep 2016	Exploring the Interplay of Software, Hardware, and ISA in Memory Model Design	Duke University	CS, ECE
33. May 2015	Accurate and Precise Translation and Compilation in the Face of Varying Memory Consistency Models	Princeton University General Examination	CS

## PRESS

OpenSSL Blog	May 2022. <a href="#">Spectre and Meltdown Attacks Against OpenSSL.</a>
TechSpot	February 2018. <a href="#">Researchers discover two new Spectre and Meltdown variants.</a>
Comm. of the ACM	December 2018. <a href="#">How to Live in a Post-Meltdown and -Spectre World.</a>
Digital Trends	February 2018. <a href="#">New 'Prime' Meltdown, Spectre exploits outlined by Nvidia, Princeton University.</a>
Gizmodo	February 2018. <a href="#">Researchers Find New Ways to Exploit Meltdown and Spectre Vulnerabilities in Modern CPUs.</a>
Hacker News	February 2018. <a href="#">MeltdownPrime, SpectrePrime: Exploiting Invalidation-Based Coherence Protocol.</a>
Tech Xplore	February 2018. <a href="#">MeltdownPrime and SpectrePrime: Researchers nail exploits.</a>
Engadget	February 2018. <a href="#">Researchers discover new ways to abuse Meltdown and Spectre flaws.</a>
Princeton University	April 2017. <a href="#">Tool for checking complex computer architectures reveals flaws in emerging design.</a>
RISC-V Organization	April 2017. <a href="#">The RISC-V Memory Consistency Model.</a>
Phys.org	News and Articles on Science and Technology. (2017). <a href="#">Tool checks computer architectures, reveals flaws in emerging design.</a>
Semiconductor Engineering	April 2017. <a href="#">System Bits: April 18 – RISC-V errors; spin-wave logic gates; deep learning is old.</a>
Electronics Weekly	April 2017. <a href="#">RISC-V bugs found by Princeton.</a>
Electronic Design	April 2017. <a href="#">Memory Ordering Flaw Found in Rare Version of RISC-V Hardware.</a>
Design and Reuse	April 2017. <a href="#">RISC-V: When a bug is really a feature.</a>

## TEACHING

Wi 2025	Instructor	CS 357S: Formal Methods for Computer Systems	Stanford
Wi 2025	Instructor	CS 256: Introduction to Automated Reasoning	Stanford
Sp 2025	Instructor	EE 282: Computer Systems Architecture	Stanford
Wi 2025	Instructor	CS 357S: Formal Methods for Computer Systems	Stanford
Wi 2025	Instructor	EE 180: Digital Systems Architecture	Stanford
Sp 2024	Instructor	EE 282: Computer Systems Architecture	Stanford
Au 2023	Instructor	CS 257: Introduction to Automated Reasoning	Stanford
Sp 2023	Instructor	EE 282: Computer Systems Architecture	Stanford
Au 2022	Instructor	CS 257: Introduction to Automated Reasoning	Stanford
Sp 2022	Instructor	EE 282: Computer Systems Architecture	Stanford

Au 2021	Instructor	CS 357S: Formal Methods for Computer Systems	Stanford
Sp 2021	Instructor	EE 180: Digital Systems Architecture	Stanford
Wi 2021	Instructor	EE 282: Computer Systems Architecture	Stanford
Au 2020	Instructor	CS 357S: Formal Methods for Computer Systems	Stanford
2016	TA	ELE/COS 375: Computer Organization and Design	Princeton
2014	TA	ELE/COS 375: Computer Organization and Design	Princeton
2012	TA	ECE 270: Introduction to Digital Systems Design	Purdue
2011	TA	ECE 270: Introduction to Digital Systems Design	Purdue