Caroline Trippel

Assistant Professor of Computer Science and Electrical Engineering, Stanford University

Stanford University
Computer Science Department
353 Serra Mall, Stanford, CA 94305

Phone: (574) 276-6171
Email: trippel@stanford.edu
Home: https://cs.stanford.edu/~trippel

EDUCATION

2013 – 2019	**Princeton University**, PhD, Computer Science Thesis: Concurrency and Security Verification in Heterogeneous Parallel Systems *(ACM SIGARCH/IEEE CS TCCA Outstanding Dissertation Award & CGS/ProQuest Distinguished Dissertation Award)* Advisor: Prof. Margaret Martonosi
2013 – 2015	**Princeton University**, MA, Computer Science
2009 – 2013	**Purdue University**, BS, Computer Engineering

PHD DISSERTATION RESEARCH

Despite parallelism and heterogeneity being around for a long time, the degree to which both are being simultaneously deployed poses grand challenge problems in computer architecture regarding ensuring the accuracy of event orderings and interleavings in system-wide executions. As it turns out, event orderings form the cornerstone of correctness (e.g., memory consistency models) and security (e.g., speculation-based hardware exploits) in modern processors. Thus, my thesis work creates formal, automated techniques for specifying and verifying the accuracy of event orderings for programs running on heterogeneous, parallel systems to improve their correctness and security.

AWARDS & HONORS

1. Jul 2023, Keynote at the 35th International Conference on Computer Aided Verification (CAV)
2. Jan 2023, NSF CAREER Award in the Division of Computing and Communication Foundations
3. 2022 Meta Research Award on Silent Data Corruption at Scale
4. 2022 DARPA Forward Riser
5. 2022: Top Picks in Hardware and Embedded Security *Shortlist* for CheckMate paper
6. 2021 VMware Early Career Faculty Grant
7. 2020 CGS/ProQuest Distinguished Dissertation Award
8. 2020 ACM SIGARCH/IEEE CS TCCA Outstanding Dissertation Award
9. 2018 IEEE MICRO Top Pick (top 12 computer architecture papers) for CheckMate paper
10. 2018 MIT Rising Stars in EECS Workshop
11. 2018 ACM Heidelberg Laureate Forum
12. 2017 IEEE MICRO Top Pick (top 12 computer architecture papers) for TriCheck paper
13. Au 2017 – Sp 2018 NVIDIA Graduate Fellowship Recipient
14. Au 2016 – Sp 2017 NVIDIA Graduate Fellowship Finalist
15. Au 2009 – Sp 2013 Richard E. Houser Trustee Scholarship in ECE (Purdue University, Full Tuition)
16. Au 2012 Michelle L. Ruth Memorial Scholarship (Purdue University)
17. Au 2012 Thomas A. Prewitt Memorial Scholarship (Purdue University)
18. Au 2012 Samuel David Williamson Scholarship (Purdue University)

19. Au 2012 Donald E. Knebel Electrical and Computer Engineering Scholarship (Purdue University)
20. Au 2012 – Sp 2013 Purdue University Dean's List
21. Sp 2011 – Sp 2013 Purdue University Semester Honors
22. 2009 Intel International Science and Engineering Fair Second Place, Minor Planet named after me by MIT Lincoln Laboratory LINEAR (URL: https://ssd.jpl.nasa.gov/sbdb.cgi#top, search "Carolinejune")

PUBLICATIONS

REFEREED

1. Daniel Mendoza, Francisco Romero, **Caroline Trippel**. "Model Selection for Latency-Critical Inference Serving". To appear in Proceedings of the 10th European Conference on Computer Systems (EuroSys), Athens, Greece. April 2024.
2. Nicholas Mosier, Hamed Nemati, John Mitchell, **Caroline Trippel**. "Serberus: Protecting Cryptographic Code from Spectres at Compile-Time". To appear in Proceedings of the 45th IEEE Symposium on Security & Privacy (S&P), San Francisco, CA. May 2024.
3. Matthias Cosler, Christopher Hahn, Daniel Mendoza, Frederik Schmitt, **Caroline Trippel**. "nl2spec: Interactively Translating Unstructured Natural Language to Temporal Logics with Large Language Models". In Proceedings of the 34th International Conference on Computer Aided Verification (CAV), Paris, France. July 2023.
4. Saranyu Chattopadhyay, Keerthikumara Devarajegowda, Bihan Zhao, Florian Lonsing, Brandon A. D'Agostino, Ioanna Vavelidou, Vijay D. Bhatt, Sebastian Prebeck, Wolfgang Ecker, **Caroline Trippel**, Clark Barrett, Subhasish Mitra. "G-QED: Generalized QED Pre-silicon Verification beyond Non-Interfering Hardware Accelerators". In Proceedings of the 60th Design Automation Conference (DAC), San Francisco, CA. July, 2023.
5. Nicholas Mosier, Hanna Lachnitt, Hamed Nemati, **Caroline Trippel**. "Axiomatic Hardware-Software Contracts for Security". In Proceedings of the 49th ACM/IEEE International Symposium on Computer Architecture (ISCA), New York, New York. June, 2022.
6. Geet Sethi, Bilge Acun, Niket Agarwal, Christos Kozyrakis, **Caroline Trippel**, Carole-Jean Wu. "RecShard: Statistical Feature-Based Memory Optimization for Industry-Scale Neural Recommendation". In Proceedings of the 27th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Lausanne, Switzerland. February-March, 2022.
7. Deeksha Dangwal, Vincent T. Lee, Hyo Jin Kim, Tianwei Shen, Meghan Cowan, Rajvi Shah, **Caroline Trippel**, Brandon Reagen, Timothy Sherwood, Vasileios Balntas, Armin Alaghi, and Eddy Ilg. "Mitigating Reverse Engineering Attacks on Local Feature Descriptors". In Proceedings of the 32nd British Machine Vision Conference (BMVC), Virtual Event. November 2021.
8. Yao Hsiao, Dominic P. Mulligan, Nikos Nikoleris, Gustavo Petri, and **Caroline Trippel**. "Synthesizing Formal Models of Hardware from RTL for Efficient Verification of Memory Model Implementations". In Proceedings of the 54th IEEE/ACM International Symposium on Microarchitecture (MICRO), Virtual Event. October, 2021.
9. Saranyu Chattopadhyayi, Florian Lonsing, Luca Piccolboni, Deepraj Soni, Peng Wei, Xiaofan Zhang, Yuan Zhou, Luca Carloni, Deming Chen, Jason Cong, Ramesh Karri, Zhiru Zhang, **Caroline Trippel**, Clark Barrett, and Subhasish Mitra. "Scaling Up Hardware Accelerator Verification using AQED with Functional Decomposition". In Proceedings of the 2021 Conference on Formal Methods in Computer Aided Design (FMCAD), Virtual Event. October 2021.
10. Jose Rodrigo Sanchez Vicarte, Pradyumna Shome, Nandeeka Nayak, **Caroline Trippel**, Adam Morrison, David Kohlbrenner, Christopher W. Fletcher. "Opening Pandora's Box: A Systematic Study of New Ways Microarchitecture Can Leak Private Data". In Proceedings of the 48th ACM/IEEE International Symposium on Computer Architecture (ISCA), Virtual Event. June 2021.

11. Meghan Cowan, Deeksha Dangwal, Armin Alaghi, **Caroline Trippel**, Vincent T. Lee, Brandon Reagen. "Porcupine: A Synthesizing Compiler for Vectorized Homomorphic Encryption". In Proceedings of the 42nd ACM SIGPLAN International Conference on Programming Language Design and Implementation (PLDI), Virtual Event. June 2021.
12. Mark Wilkening, Udit Gupta, Samuel Hsia, **Caroline Trippel**, Carole-Jean Wu, David Brooks, and Gu-Yeon Wei. "RecSSD: Near Data Processing for Solid State Drive Based Recommendation Inference". In Proceedings of the 26th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Virtual Event. April 2021.
13. Kiwan Maeng, Shivam Bharuka, Isabel Gao, Mark Jeffrey, Vikram Saraph, Bor-Yiing Su, **Caroline Trippel**, Jiyan Yang, Mike Rabbat, Brandon Lucia, and Carole-Jean Wu. "Understanding and Improving Failure Tolerant Training for Deep Learning Recommendation with Partial Recovery". In Proceedings of the 3rd Conference on Machine Learning and Systems (MLSys), Virtual Event. April 2021.
14. Deeksha Dangwal, Meghan Cowan, Armin Alaghi, Vincent T Lee, Brandon Reagen, and **Caronline Trippel**. "SoK: Opportunities for Software-Hardware-Security Codesign for Next Generation Secure Computing". In Proceedings of the 9th ACM Workshop on Hardware and Architectural Support for Security and Privacy (HASP), Virtual Event. October 2020.
15. Naorin Hossain, **Caroline Trippel**, and Margaret Martonosi. "TransForm: Formally Specifying Transistency Models and Synthesizing Enhanced Litmus Tests". In Proceedings of the 47th ACM/IEEE International Symposium on Computer Architecture (ISCA), Virtual Event. May-June 2020. Acceptance rate: 77/421=18.3%.
    Presents an axiomatic vocabulary for formally specifying "transistency models" and a tool for synthesizing litmus tests enhanced with transistency features, when supplied with a formal transistency model specification.
16. **Caroline Trippel**, Daniel Lustig, and Margaret Martonosi. "Security Verification through Automatic Hardware-Aware Exploit Synthesis: The CheckMate Approach". IEEE Micro, 39 (3), May-June 2018. Issue: Top Picks from the Computer Architecture Conferences of 2018.
    Makes the important observation that MCM analysis is in many ways similar to hardware security analysis, paving the way for fresh approaches to security specification and verification in the hardware-software stack.
17. Hongce Zhang, **Caroline Trippel**, Yatin A. Manerkar, Aarti Gupta, Margaret Martonosi, and Sharad Malik. "Integrating Memory Consistency Models with Instruction-Level Abstractions for Heterogeneous System-onChip Verification". In Proceedings of the 2018 Conference on Formal Methods in Computer Aided Design (FMCAD), Austin, Texas. October-November 2018.
    New approach for integrating axiomatic memory consistency model specifications with operational specifications of heterogeneous SoC components to reason about overall system behavior
18. **Caroline Trippel**, Daniel Lustig, and Margaret Martonosi. "CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests". In Proceedings of the 51st IEEE/ACM International Symposium on Microarchitecture (MICRO), Fukuoka, Japan. October 2018. Acceptance rate: 74/351=21.0%.
    Approach and automated tool for evaluating microarchitectural susceptibility to exploit classes and synthesizing proof-of-concept exploit code; out-of-the-box CheckMate synthesized Meltdown, Spectre and new attacks.
19. **Caroline Trippel**, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. "Full-Stack Memory Consistency Model Verification with TriCheck". IEEE Micro, 38 (3), May-June 2018. Issue: Top Picks from the Computer Architecture Conferences of 2017.
    First full-stack language/ISA/microarchitecture memory consistency model verification tool, which uncovered concrete and fundamental problems in the C11/C++11 and RISC-V memory models.
20. **Caroline Trippel**, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. "TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA". In Proceedings of the 22nd ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Xi'an, China. April 2017. Acceptance rate: 56/321=17.4%

Established the value of full-stack memory consistency model verification and highlighted issues with the RISC-V memory model that were subsequently fixed through the RISC-V Memory Model Working Group.

21. Daniel Lustig, **Caroline Trippel**, Michael Pellauer, and Margaret Martonosi. "ArMOR: Defending Against Memory Consistency Model Mismatches in Heterogeneous Architectures". In Proceedings of the 42nd ACM/IEEE International Symposium on Computer Architecture (ISCA), Portland, Oregon. June 2015. Acceptance rate: 58/305=19.0%.
Framework that supports specifying, algorithmically reasoning about, and automatically translating between heterogenous MCMs.

NON-REFEREED / NON-PROCEEDINGS

1. Chuyue Sun, Christopher Hahn, and **Caroline Trippel**. "Towards Improving Verification Productivity with Circuit-Aware Translation of Natural language to SystemVerilog Assertions". 1st International Workshop on Deep Learning-aided Verification (DAV), Paris, France. July 2023.
2. Nicholas Mosier, Kate Eselius, Hamed Nemati, John Mitchell, and **Caroline Trippel**. "Hardware-Software Codesign for Mitigating Spectre". 1st Workshop on Programming Languages for Architecture (PLARCH), Orlando, FL. June 2023.
3. Yao Hsiao, Yasas Seneviratne, Tommy Tracy II, Kevin Skadron, and **Caroline Trippel**. "Design for Hardware Memory Model Verification". 1st Workshop on Programming Languages for Architecture (PLARCH), Orlando, FL. June 2023.
4. Paul Mure, Nathan Zhang, **Caroline Trippel**, Kunle Olukotun. "Tags: A Framework for Distributed Event Ordering". 1st Workshop on Programming Languages for Architecture (PLARCH), Orlando, FL. June 2023.
5. Daniel Mendoza and **Caroline Trippel**. "Dynamic Network Adaptation at Inference". arXiv, abs/2204.08400. April 2022.
6. Daniel Mendoza and **Caroline Trippel**. "SLO-NNs: Service Level Objective-Aware Neural Networks". 2nd European Workshop on Machine Learning and Systems (EuroMLSys), Rennes, France. April 2022.
7. Nicholas Mosier, Hanna Lachnitt, Hamed Nemati, and **Caroline Trippel**. "Relational Models of Microarchitectures for Formal Security Analyses". arXiv, abs/2112.10511. December 2021.
8. Deeksha Dangwal, Vincent T Lee, Hyo Jin Kim, Tianwei Shen, Meghan Cowan, Rajvi Shah, **Caroline Trippel**, Brandon Reagen, Timothy Sherwood, Vasileios Balntas, Armin Alaghi, and Eddy Ilg. "Analysis and Mitigations of Reverse Engineering Attacks on Local Feature Descriptors". arXiv, abs/2105.03812. December 2021.
9. **Caroline Trippel**, Daniel Lustig, and Margaret Martonosi. "MeltdownPrime and SpectrePrime: Automatically-Synthesized Attacks Exploiting Invalidation-Based Coherence Protocols". arXiv, abs/1802.03802. February 2018.
Overview of MeltdownPrime and SpectrePrime exploits that were automatically synthesized by CheckMate and which were demonstrated to leak private data on Intel hardware.
10. Yatin A. Manerkar, **Caroline Trippel**, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. "Counterexamples and Proof Loophole for the C/C++ to POWER and ARMv7 Trailing-Sync Compiler Mappings". arXiv, abs/1611.01507. November 2016.
Identification of an error in a compiler mapping proof from C11 to the IBM Power and ARMv7 ISAs; the error is what enabled TriCheck to identify concrete compiler mapping counterexamples.
11. **Caroline Trippel**, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. "Exploring the Trisection of Software, Hardware, and ISA in Memory Model Design". arXiv, abs/1608.07547. August 2016.

DISSERTATIONS

1. **Caroline Trippel**. "Concurrency and Security Verification in Heterogeneous Parallel Systems." PhD Dissertation. Princeton University. November 2019.

TUTORIALS

1. Yatin A. Manerkar, **Caroline Trippel**, and Margaret Martonosi. "Demystifying Memory Models Across The Computing Stack." Tutorial. 46th ACM/IEEE International Symposium on Computer Architecture (ISCA), Phoenix, Arizona. June 2019.
2. **Caroline Trippel** and Yatin A. Manerkar. "Why Memory Consistency Models Matter... And tools for analyzing and verifying them." Tutorial. 2018 Uppsala Programming for Multicore Architectures Research Center (UPMARC) Multicore Computing Summer School, Uppsala, Sweden. June 2018.
3. Yatin A. Manerkar, **Caroline Trippel**, and Margaret Martonosi. "Why Memory Consistency Models Matter... And tools for analyzing and verifying them." Tutorial. 44th ACM/IEEE International Symposium on Computer Architecture (ISCA), Toronto, Ontario, Canada. June 2017.

BLOG POSTS

1. **Caroline Trippel**. Interactively Translating Unstructured Natural Language to Temporal Logics with nl2spec. SIGARCH Blog. June, 2023.
2. **Caroline Trippel**. Silent Data Corruption at Scale. SIGARCH Blog. August, 2022.
3. **Caroline Trippel**. Applications of Formal Methods in Computer Architecture." SIGARCH Blog. Sept., 2021.
4. **Caroline Trippel**. The Academic Job Search: A Memoir, Part 2. SIGARG Blog, December, 2020.
5. **Caroline Trippel**. The Academic Job Search: A Memoir. SIGARCH Blog. December, 2020.
6. **Caroline Trippel**. Reflections on the ISCA Mini-Panel on Security. SIGARCH Blog. August, 2020.

PRESS

OpenSSL Blog	May 2022. Spectre and Meltdown Attacks Against OpenSSL.
TechSpot	February 2018. Researchers discover two new Spectre and Meltdown variants.
Comm. of the ACM	December 2018. How to Live in a Post-Meltdown and -Spectre World.
Digital Trends	February 2018. New 'Prime' Meltdown, Spectre exploits outlined by Nvidia, Princeton University.
Gizmodo	February 2018. Researchers Find New Ways to Exploit Meltdown and Spectre Vulnerabilities in Modern CPUs.
Hacker News	February 2018. MeltdownPrime, SpectrePrime: Exploiting Invalidation-Based Coherence Protocol.
Tech Xplore	February 2018. MeltdownPrime and SpectrePrime: Researchers nail exploits.
Engadget	February 2018. Researchers discover new ways to abuse Meltdown and Spectre flaws.
Princeton University	April 2017. Tool for checking complex computer architectures reveals flaws in emerging design.
RISC-V Organization	April 2017. The RISC-V Memory Consistency Model.
Phys.org	News and Articles on Science and Technology. (2017). Tool checks computer architectures, reveals flaws in emerging design.
Semiconductor Engineering	April 2017. System Bits: April 18 – RISC-V errors; spin-wave logic gates; deep learning is old.
Electronics Weekly	April 2017. RISC-V bugs found by Princeton.
Electronic Design	April 2017. Memory Ordering Flaw Found in Rare Version of RISCV Hardware.
Design and Reuse	April 2017. RISC-V: When a bug is really a feature.

PROFESSIONAL EXPERIENCE

2020 –	**Assistant Professor**, Department of Computer Science and Department of Electrical Engineering	**Stanford University**, Stanford, CA
2019 – 2020	**Research Scientist**, FAIR SysML Manager: Hsien-Hsien Lee	**Facebook**, Boston, MA
2013 – 2019	**PhD Student**, Computer Science Department Advisor: Margaret Martonosi	
2016	**Graduate Research Intern**, Architecture Research Group Supervisor: Steve Keckler Mentor: Michael Pellauer	**NVIDIA**, Westford, MA
2015	**Graduate Research Intern**, Architecture Research Group Supervisor: Steve Keckler Mentor: Michael Pellauer	**NVIDIA**, Westford, MA
2013	**Verification Graduate Intern**, P-Series Verification Group Supervisor: David A. King	**IBM**, Austin TX
2012	**Undergraduate Technical Intern**, FEV/DFT Group Supervisor: Sulakshana Nath	**Intel**, Hillsboro, OR
2011	**Continuous Improvement Intern** Supervisor: Chris Young	**Blue Cross Blue Shield**, Providence, RI

INVITED TALKS

KEYNOTES

Jul 2023	Verified Software Security Down to Gates	35th International Conference on Computer Aided Verification (CAV), Paris, France.	Hosts: Constantin Enea, Akash Lal

SPRING 2019 SEMINAR

Concurrency and Security Verification in Heterogeneous Parallel Systems

University of California, Berkeley
Carnegie Mellon University
Cornell University
Cornell Tech
Duke University
Northeastern University
Tufts University
University of California, Santa Barbara
University of Illinois Urbana-Champaign
Columbia University
Stanford University
University of Washington
Yale University
University of Pennsylvania
Brown University
University of Wisconsin-Madison
University of Texas at Austin
Microsoft

SEMINARS & TALKS

Jul 2023	System-Level Testing for Silent Data Corruptions	Open Compute Project Bi-Weekly Meeting, Virtual.	Host: Bharath Parthasarathy
Jun 2023	Uncovering Transmitter Instructions on the RISC-V CVA6 Processor	7th Workshop on Computer Architecture Research with RISC-V (CARRV), at ISCA 2023, Orlando, FL.	Host: Trevor Carlson
Jun 2023	Scalable Assurance via Verifiable Hardware-Software Contract	Council on Electronic Design Automation (CEDA) Hong Kong Chapter, 2023 Seminar Series, Virtual.	Host: Hongce Zhang
May 2023	Scalable Assurance via Verifiable Hardware-Software Contracts	Intel Scalable Assurance Spring Workshop, Virtual.	
Mar 2023	Searching for Bugs in Real Computer Systems	Women in Computer Architecture (WICARCH) Seminar, Virtual.	
Feb 2023	Scalable Assurance via Verifiable Hardware-Software Contracts	Intel IPAS Tech Sharing Seminar, Virtual.	Host: Sayak Ray
Feb 2023	Scalable Assurance via Verifiable Hardware-Software Contracts	Workshop on Security for Custom Computing Machines (SCCM), at FPGA 2023, Virtual.	Hosts: Dustin Richmond, Ryan Kastner, Jeff Goeders, Mirjana Stojillović
Jan 2023	Scalable Assurance via Verifiable Hardware Software Contracts	Stanford Engineering Research Introductions (SERIS) Program, Stanford, CA.	
Nov 2022	System-Level Testing for Silent Data Corruptions	AMD, Virtual.	Host: Sudhanva Gurumurthi
Nov 2022	Microarchitectural Attack Synthesis with Happens-Before Analysis	Top Picks in Hardware and Embedded Security Workshop, ICCAD 2022, San Diego, CA.	
Sep 2022	Scalable Assurance via Formal and Verifiable Hardware-Software Contracts	Intel Scalable Assurance Fall Workshop, Hillsboro, OR.	
Aug 2022	System-Level Testing for Silent Data Corruptions	2022 Google Accelerators, Compute, Reliability, Security (ACRS) Workshop, Virtual.	Host: Parthasarathy Ranganathan
Jul 2022	Scalable Assurance via Formal and Verifiable Security Contracts	Center for Automated Reasoning (CENTAUR) at Stanford University, Annual Meeting, Stanford, CA.	Host: Clark Barrett
Jun 2022	System-Level Testing for Silent Data Corruptions	Google, Virtual.	Host: Bharath Parthasarathy
Apr 2022	Scalable Assurance via Formal and Verifiable Hardware-Software Contracts	Berkeley Security Seminar, Virtual.	

Mar 2022	Axiomatic Hardware-Software Contracts for Security	IMDEA Invited Talk, with Nicholas Mosier and Hanna Lachnitt, Virtual.	Host: Marco Guanieri
Nov 2021	Formally Verifying Hardware with Happens-Before Analysis	2021 Stanford SystemX Fall Conference, Virtual.	
Oct 2021	Synthesizing Formal Models of Hardware from RTL for Efficient Hardware Memory Model and Security Verification	AHA Affiliates Meeting, Virtual.	Host: Priyanka Raina, Mark Horowitz
Oct 2021	Automatically Synthesizing Formal Processor Models from RTL for Scalable Hardware Security Verification	Intel Scalable Assurance Program Kickoff, Virtual	
Sep 2021	Application Correctness and Security via Formal Methods for Systems	VMWare, Virtual.	Host: Jayneel Gandhi
Sep 2021	Formally Evaluating Microarchitectural Security with Happens-Before Analysis	Stanford Security Forum, Stanford, CA.	Host: Dan Boneh, Zakir Durumeric
Aug 2021	Searching for Bugs in Real Computer Systems	Cross-layer Computing Summer School: Circuits to System, Evanston, IL.	Host: Jie Gu, Russ Joseph, Seda Memik, Qi Zhu
Jun 2021	Application Correctness & Security via Formal Methods for Systems	Apple, Virtual.	Host: Abhishek Datta
Jun 2021	Application Correctness & Security via Formal Methods for Systems	Intel Labs University Research and Collaboration Group, Virtual.	
May 2021	Application Correctness & Security via Formal Methods for Systems	Stanford Systems Seminar, Virtual.	
Apr 2021	Searching for Bugs in Real Computer Systems	Workshop on Negative results, Opportunities, Perspectives, and Experiences, at ASPLOS 2021, Virtual.	Hosts: Lillie Pentecost, Udit Gupta, David Brooks, Brandon Reagen, Svilen Kanev, Bob Adollf
Apr 2021	Verifying Correctness and Security of Hardware though Event Orderings	Guest Lecture in Brown's Logic for Systems Course, Virtual.	Host: Timothy Nelson
Jan 2021	Concurrency and Security Verification in Heterogeneous Parallel Systems	Phil Harper Lapidus Lecture/CGS Awards Ceremony, Virtual.	
Dec 2020	Application Security via Formal Methods for Systems	Stanford Security Lunch, Virtual.	
Nov 2020	Lifting Axiomatic Hardware Specifications from RTL for Security Analysis	Intel Side-Channel Academic Program (SCAP) Fall Workshop, Virtual.	
Nov 2020	Application Reliability and Security via Formal Methods for Systems	2020 Stanford SystemX Fall Conference, Virtual.	
Oct 2020	My Academic Interview Tips	JOBS Workshop, at MICRO 2020, Virtual.	

Aug 2020	Application Reliability and Security via Formal Methods for Systems	2020 Annual Meeting, Stanford Computer Forum, New Research Directions in CS Session, Virtual.	
Oct 2019	Concurrency and Security Verification in Heterogeneous Parallel Systems	Talk	Princeton University Preliminary Final Public Oral, Princeton, NJ.
Sep 2019	CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests	2019 Arm Summit, Austin, TX.	
Sep 2019	Synthesizing Security Exploits	2019 State-of-the-Art in Program Synthesis Workshop, San Francisco, CA.	Hosts: Saurabh Srvastava, Ratislav Bodik
Nov 2018	Concurrency and Security Verification in Heterogeneous Parallel Systems	2018 IBM Workshop on Architectures for Secure, Cognitive, and Datacenter Computing, Yorktown, NY.	Hosts: Michael Healy, Arvind Kumar
Nov 2018	Concurrency and Security Verification in Heterogeneous Parallel Systems	MIT CSAIL, Cambridge, MA.	Host: Saman Amarasinghe
Oct 2018	CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests	51st International Symposium on Microarchitecture (MICRO), Fukuoka, Japan.	
Mar 2018	Automated Exploit Program Generation for Hardware Security Verification	Apple Security Engineering and Architecture Group, Cupertino, CA.	Host: Ivan Krstić
Mar 2018	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	Brown University Computer Science Department, Providence, RI.	Host: Iris Bahar, Mauric Herlihy
Mar 2018	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	NVIDIA GPU Technology Conference (GTC), San Jose, CA.	
Apr 2017	TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA	22nd International Conference on Architectural Support for Programming languages and Operating Systems (ASPLOS), Xian, China.	
Sep 2017	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	SRC TECHCON 2017, Austin, Texas.	
Jul 2017	Why Memory Consistency Models Matter in a World of Parallelism and Shared Memory	Rutgers University DIMACS Research Experiences for Undergraduates, New Brunswick, NJ.	Host: Lazaros Gallos
Nov 2016	A Memory Consistency Model for RISC-V	5th RISC-V Workshop, Google, Mountain View, CA	

Nov 2016	TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA	SRI International, Menlo Park, CA.	Host: Prashanth Mundkur
Sep 2016	Exploring the Interplay of Software, Hardware, and ISA in Memory Model Design	Duke University Computer Science/Electrical Computer Engineering, Durham, NC.	Host: Benjamin Lee
Sep 2016	Memory Consistency Model Aware ISA Design and Specification	SRC TECHCON 2016, Austin, Texas.	
May 2015	Accurate and Precise Translation and Compilation in the Face of Varying Memory Consistency Models	Princeton University General Examination, Princeton, NJ	

OTHER PRESENTATIONS

Jun 2023	Round Table on Implications for the Design and Validation of Secure Systems	Panelist	Seventh Workshop on Computer Architecture Research with RISC-V (CARRV), at ISCA 2023, Orlando, FL.
Dec 2022	Scalable Assurance via Formal and Verifiable Hardware- Software Contracts	Poster	DARPA Risers Workshop at 2022 DARPA Forward Conference, San Diego, CA.
Jun 2022	Panel on Silent Data Corruption	Panelist	ISCA 2022, New York, NY.
Jun 2020	Security Mini-Panel	Panelist	ISCA 2020, Virtual.
Oct 2018	CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests	Poster	51st International Symposium on Microarchitecture (MICRO), Fukuoka, Japan.
Sep 2018	Concurrency and Security Verification in Heterogeneous Parallel Systems	Poster	Heidelberg Laureate Forum, Heidelberg, Germany.
Mar 2018	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	Poster	NVIDIA GPU Technology Conference (GTC), San Jose, CA.
Sep 2017	Relational Model Finding for Hardware-Aware Program Synthesis and Security Verification	Poster	SRC TECHCON 2017, Austin, Texas.
Apr 2017	TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA	Poster	22nd International Conference on Architectural Support for Programming languages and Operating Systems (ASPLOS), Xian, China.
Sep 2016	Memory Consistency Model Aware ISA Design and Specification	Poster	SRC TECHCON 2016, Austin, Texas.
Apr 2016	Design Space Exploration Techniques for Memory Consistency Model Aware ISA Specification	Poster	CRA-W Grad Cohort, San Diego, California.
Dec 2015	ArMOR: Defending Against Memory Consistency Model Mismatches in Heterogeneous Architectures	Poster	2nd Career Workshop for Women and Minorities in Computer Architecture, Honolulu, Hawaii.

STUDENT ADVISING

POSTDOCTORAL

Au 2022 – Au 2023	Christopher Hahn	Stanford CS
Sp 2021 – Sp 2023	Hamed Nemati	Stanford CS

PHD

Su 2023 –	Colin Drewes	Stanford CS
Su 2022 –	Ioanna Vavelidou	Stanford EE
Su 2022 –	Daniel Mendoza	Stanford EE
Su 2022 – Sp 2023	Brandon D'Agostino	Stanford EE
Wi 2022 –	Rachel Cleaveland	Stanford CS
Au 2021 –	Yao Hsiao	Stanford EE
Au 2021 –	Saranyu Chattopadhyay	Stanford EE
Sp 2021 – Su 2021	Geet Sethi	Stanford CS
Su 2021 –	Nicholas Mosier	Stanford CS
Au 2020 – Sp 2022	Hanna Lachnitt	Stanford CS

PHD ROTATIONS

Au 2023	Samantha Archer	Stanford EE
Wi 2023	Livia Sun	Stanford CS
Wi 2023	Áron Ricardo Perez-Lopez	Stanford CS
Au 2022	Colin Drewes	Stanford CS
Su 2022	Brandon D'Agostino	Stanford EE
Sp 2022	Ioanna Vavelidou	Stanford EE
Wi 2022	Rachel Cleaveland	Stanford CS
Au 2021	Obi Nnorom	Stanford EE
Au 2021	Daniel Mendoza	Stanford EE
Wi 2021	Nicholas Mosier	Stanford CS
Au 2021	Yao Hsiao	Stanford EE

MASTERS

Wi 2023	Bay Foley-Cox	Stanford CS
Au 2022 – Sp 2023	Paul Mure	Stanford CS
Au 2020 – Su 2021	Saranyu Chattopadhyay	Stanford EE
Au 2021 – Sp 2022	Sanjana Sarda	Stanford EE
Wi 2021 – Sp 2022	George Klimiashvili	Stanford EE
Wi 2021 – Sp 2022	Sneha Pendharkar	Stanford EE
Au 2020 – Su 2021	Yao Hsiao	Stanford EE
Au 2020 – Sp 2021	Eldrick Millares	Stanford EE

UNDERGRADUATE

Au 2022 –	Kate Eselius	Stanford CS
Au 2022 – Sp 2023	Devrath Iyer	Stanford EE
Au 2022 – Sp 2023	Evan Cheng	Stanford CS
Au 2021 – Sp 2022	Paul Mure	Stanford CS
Wi 2021 – Sp 2022	Nandita Naik	Stanford CS

ORAL DEFENSE COMMITTEES

Jan 2024	Sneha Geonka	Advisor: Mark Horowitz	Stanford EE	Examiner	Biology needs Computer Architects: Keeping up with genomic-scale data
May 2023	Francisco Romero	Advisor: Christos Kozyrakis	Stanford EE	Examiner (Reader)	General Purpose and Interactive Video Analytics
May 2023	Ruby Shi	Advisor: Kathryn Moler	Stanford, Physics	Chair	Magnetic Imaging of Two-Dimensional Superconductors with Scanning SQUID Microscopy
May 2023	Wonyeol Lee	Advisor: Alex Aiken	Stanford CS	Examiner	Reasoning about Floating Point in Real-World Systems
Apr 2023	Qian Li	Advisor: Christos Kozyrakis	Stanford CS	Examiner (Reader)	Abstractions for Efficient and Reliable Serverless Computing
Dec 2022	Geet Sethi	Advisor: Christos Kozyrakis	Stanford CS	Examiner (Reader)	Data-Driven Statistical Sharding for Industry-Scale Neural Recommendation
Feb 2022	Jason Koenig	Advisor: Alex Aiken	Stanford CS	Examiner (Reader)	Invariant Inference via Quantified Separation, Dissertation Reader
Jun 2021	Makai Mann	Advisor: Clark Barrett	Stanford CS	Examiner (Reader)	Augmenting Transition Systems for Scalable Symbolic Model Checking

QUALIFYING EXAM COMMITTEES

Aug 2023	Nicholas Mosier	Advisor: Caroline Trippel	Stanford CS
Jun 2023	Ioanna Vavelidou	Advisor: Caroline Trippel	Stanford EE
Jun 2023	Kimberly Ruth	Advisor: Zakir Durumeric	Stanford CS
Jun 2023	Rubens Lacouture	Advisor: Kunle Olukotun	Stanford EE
Mar 2023	Daniel Mendoza	Advisor: Caroline Trippel	Stanford EE
Mar 2023	Amalee Wilson	Advisor: Clark Barrett	Stanford CS
Feb 2023	Yao Hsiao	Advisor: Caroline Trippel	Stanford EE
Feb 2023	Saranyu Chattopadhyay	Advisor: Subhasish Mitra	Stanford EE
Nov 2022	Ying Sheng	Advisor: Clark Barrett	Stanford CS
May 2022	Po-Han Chen	Advisor: Priyanka Raina	Stanford EE
Apr 2022	Alex Oxdemir	Advisor: Clark Barrett, Dan Boneh	Stanford CS
Feb 2022	Athinagoras Skidadopoulos	Advisor: Christos Kozyrakis	Stanford EE

TEACHING

Au 2023	Instructor	CS 257: Introduction to Automated Reasoning	Stanford
Sp 2023	Instructor	EE 282: Computer Systems Architecture	Stanford
Au 2022	Instructor	CS 257: Introduction to Automated Reasoning	Stanford
Sp 2022	Instructor	EE 282: Computer Systems Architecture	Stanford
Au 2021	Instructor	CS 357S: Formal Methods for Computer Systems	Stanford
Sp 2021	Instructor	EE 180: Digital Systems Architecture	Stanford
Wi 2021	Instructor	EE 282: Computer Systems Architecture	Stanford
Au 2020	Instructor	CS 357S: Formal Methods for Computer Systems	Stanford
2016	TA	ELE/COS 375: Computer Organization and Design	Princeton
2014	TA	ELE/COS 375: Computer Organization and Design	Princeton
2012	TA	ECE 270: Introduction to Digital Systems Design	Purdue
2011	TA	ECE 270: Introduction to Digital Systems Design	Purdue

PROFESSIONAL SERVICE

TECHNICAL PROGRAM COMMITTEES

2023	ASPLOS 2024	TPC
2023	IEEE Micro Top Picks 2023	TPC
2022	HPCA 2023	ERC
2022	ASPLOS 2023	TPC
2021	MLSys 2022	TPC
2021	ASPLOS 2022	TPC
2021	ISCA 2021	TPC
2021	IEEE Micro Top Picks 2021	TPC
2020	ASPLOS 2021	TPC
2020	ISCA Industry Tack 2020	TPC
2019	ASPLOS 2020	TPC
2019	MICRO 2019	TPC

OTHER TECHNICAL REVIEWING

2022	OSDI 2022	Expert Reviewer
2018	International Symposium on Memory Management	Expert Reviewer
2018	Principles of Secure Processor Architecture Design by Jakub Szefer, a Morgan & Claypool Synthesis Lecture on Computer Architecture	Expert Reviewer

OTHER SERVICE

2024	Young Architects Workshop (YArch) 2023, Co-Organizer
2023	Dagstuhl Seminar 23481, “MAD: Microarchitectural Attacks and Defenses”, Participant.
2023	2023 ACM Student Research Competition (SRC), Co-chair, at MICRO 2023, Toronto, Canada.

2023	2023 Undergrad Architecture Mentoring Workshop, In-person mentor, at ISCA 2023, Orlando, Florida.
2022	2022 Berkeley/Stanford/UCSC Cloud Workshop. Co-organizer, part of the Industry-Academia Partnership.
2022	Wild and Crazy Ideas (WACI) Workshop, Co-organizer, at ASPLOS 2022, Lausanne, Switzerland.
2022	NSF CISE/CCF workshop "Redefining the Future of Computer Architecture from First Principles (Arch-1)", Participant (1/~31).
2021	Workshops and Tutorials, Co-chair, at ASPLOS 2021, Virtual.
2020	DARPA/ISAT study "DOPLR: Data-Oblivious Interdisciplinary Representation", Participant (1/~45).
2016	Dagstuhl Seminar 16471, "Concurrency with Weak Memory Models: Semantics, Languages, Compilation, Verification, Static Analysis, and Synthesis", Participant.

PROFESSIONAL MEMBERSHIPS

1. ACM Member, ACM SIGARCH
2. IEEE Member
3. RISC-V Memory Model Working Group *(past)*
4. SWE Student Member, Society of Women Engineers *(past)*
5. PWICS Member, Princeton Women in Computer Science *(past)*

RELEVANT TECHNICAL COURSEWORK

Computer Architecture, Parallel Computation, Programming Languages, Advanced Computer Networks, Computer Design and Prototyping, Digital Systems Senior Design, Introduction to Compilers and Translation Engineering, Microprocessor Systems and Interfacing, ASIC Design

ENVIRONMENTS, LANGUAGES, & DESIGN TOOLS EXPERIENCE

UNIX, LINUX, CUDA, MPLAB, MATLAB, Alloy, Perl, Python, Korn Shell, C, C++, Assembly, Abel, JavaScript, Visual Basic, HTML, C#, SQL, VHDL, Verilog, Java, PSPICE, ModelSim, CodeWarrior, Pin, DynamoRIO, gem5, JasperGold